IDEC Chip Design Contest

Fully digital and Adaptive External Delay Control Circuit for MV – HEVC

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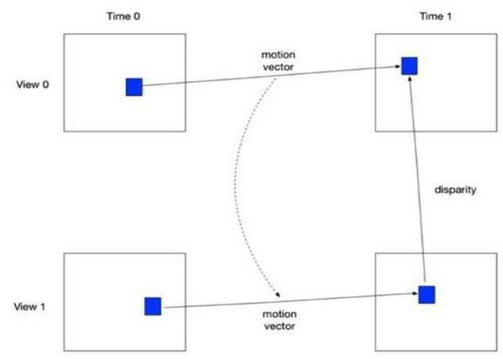
ABSTRACT

- This study proposed a system that uses more than Mb size memory even in very small environment such as MV-HEVC. Instead of using memory inside the chip, it uses external memory, especially memory such as DDR1, which can operate at low speeds. IO is not specially designed for memory use, but to allow memory access using GPIO. Low power delay is implemented to control skew between data and memory control that can operate at low speed. The implementation of the algorithm made the chip through **the Samsung 65nm foundry process.**

BACKGROUND

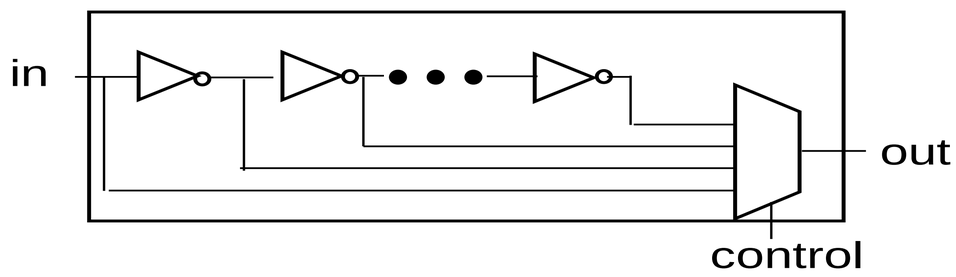
MV - HEVC



- MV HEVC is a videio coding technique using Multiview. As shown in Figure 1, MV HEVC has multiple sequences of information unlike HEVC, so it is not only necessary to estimate motion of the time axis, but also essential to estimating the motion of the space axis
- When the image data enters the bit-stream, it is processed through the entropy Decoder and then buffered again before processing IDCT, Motion Composition. The image data processed in such a way is eventually restored via Deblocking and SAO. High capacity memory is essential for intermediate storage of image data here.

Fig. 1 Motion estimation of MV – HEVC

Delay Control Unit



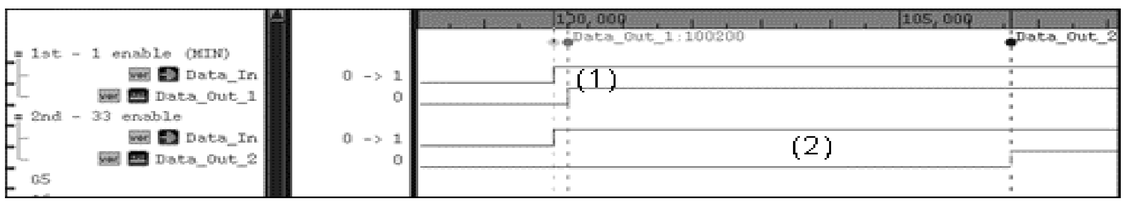


Fig. 2 Interface Control Block Diagram

- **Delay cell** was added as shown in Figure to solve the timing violation, which can occur even in the same data input in real chip operation. This can be controlled using a total of 128 layers and adjusted up to 40 ns.
- In this Chip, **I2C Slave** were designed inside simultaneously to control registers that required initial setting and monitor the condition of the chip according to the situation.

Memory Control Unit

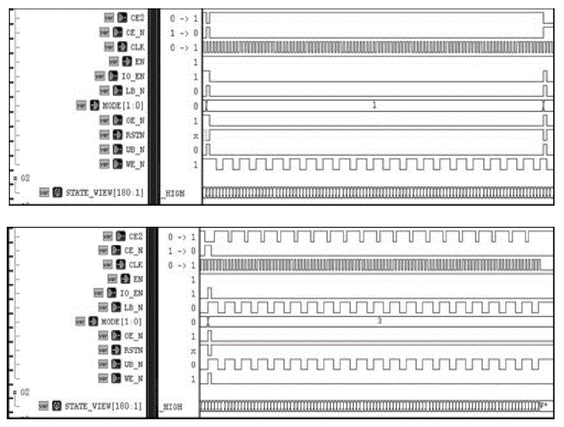


Fig. 3. Memory Read & Write Simulation

- In the decoding process, there are many limitations of capacity to perform computations using internal memory. Therefore, external memory was used to solve this problem and the **SRAM controller** was designed to control it.

RESULT

Delay Cell

Table 1 Delay Cell Size

Unit	Synthesis	Place & Route
Unit Delay cell	10.24 um^2	13.312 um^2
Memory Control	276.48 um^2	365.23 um^2
Delay Control	792.32 um^2	117.1712 um^2

Table 2 compare delay step

This work	This Work	[4]
Process	65 nm	130 nm
Period	200 ps	340 ps

Fig. 4. Delay Cell Table

- Table 1 shows the composite size of the delay cell and the p & r size of the actual chip. The unit delay cell is the size of the cell used for the two inverters and mux. The memory controller is the sum of the sizes of some flip-flops and debugging operations inside. Delay control includes logic to add and subtract blocks and other delays that determine the edge.

Interface Control Block

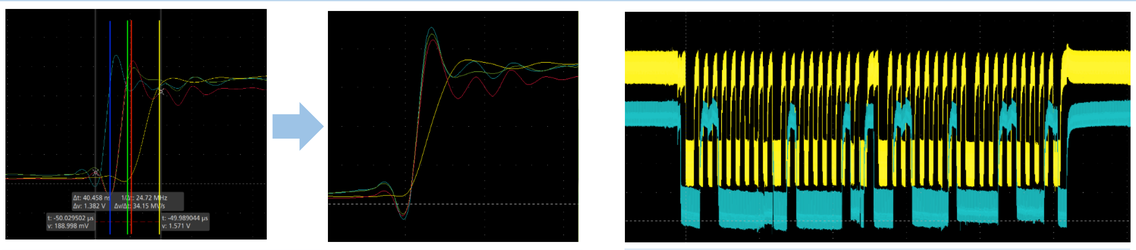


Fig. 5.1. & 5.2. Simulation of Delay Cell

Fig. 5.3.Wave of I2C

- Figure 5.1 shows that the signals to be of the same timing are in different states before the delay cell is applied. The difference between the fastest and slowest signals is about 40 ns, which means that if the operating frequency is 25Mhz, it is pushed out by one clock. Therefore, to address this, it is necessary to properly control the 128 steps of the delay cell with I2C to arrange the same timing as shown in Figure 5.2.

CONCLUSION

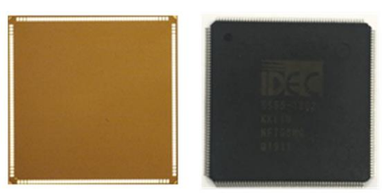


Fig. 6. chip

- HEVC is widely used in mobile and other industries. In particular, demand for MV-HEVCs is increasing on mobile platforms. However, MV-HEVC, implemented in standard C++, is not suitable for mobile platforms and needs to be implemented with hardware. so we used HLS to implement it as hardware, then expanded to ASIC.
- Initial functions required during MV-HEVC checks were controlled using i2c, which resulted in significant pin reduction. It also facilitated control of various blocks of detail, such as delay cell control, MUX, and external setting.

ACKNOWLEDGE

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